

Designing with Super Capacitors

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A growing number of battery-based portable systems today are adding functions that require very high, but instantaneous pulses of power. These loads often demand high peak currents that pose serious design challenges in systems where the average available current is limited. More and more often designers are being asked to find new ways to meet these high load demands without exceeding the capability of the host power supply.

Some of the best examples of these applications can be found in the many wireless data cards used for GSM, GPRS, TD-CDMA or WiMax data communications. Based on TDMA techniques, these wireless protocols typically require a high peak current during their transmission phase and a significantly lower current during their receiving phase. A GSM power amplifier, for example, demands a peak current as high as 2A during transmit, while needing only about 100 mA during the receive phase. To compensate for this wide range, designers typically “average” the current drawn from the supply by using capacitors to store the energy during the off period and releasing the peak current when needed.

If designers used conventional capacitor technology to solve this problem, they would need to use an extremely large cap size or connect multiple capacitors in parallel. Instead, they typically reduce the size of the solution by using very high value “super” capacitors which exhibit a high capacitance in a relatively small case size.

Multiple Challenges

A number of unique design challenges crop up when using super capacitors; A capacitor is basically two parallel conducting plates separated by an insulating material known as a dielectric. The value of the capacitor is directly proportional to the area of the plates and inversely proportional to the thickness of the dielectric:

$$C = \epsilon \frac{A}{D} \text{ farads (F)}$$

Where: C = capacitance, ϵ = overall permittivity in farads/meter, A = area of the plates and D the thickness of the dielectric.

Manufacturers of super capacitors achieve these high values of capacitance, while at the same time minimizing the size, using a porous carbon material for the plates, to maximize the surface area, while using a molecularly thin electrolyte as the dielectric, to minimize the distance between the plates. This allows them to manufacture capacitors with values starting from as little as 16mF up to a massive 2.3F.

The super capacitor construction also results in a low internal resistance (esr), making them ideal for delivering high peak current pulses without too much droop in the output voltage. One disadvantage is that the cell voltage is around 2.2V -2.5V which means for many applications cells have to be put in series. Depending upon the type and manufacturer this could mean having to add cell balancing to ensure that the cells share the voltage equally.

While a super capacitor's low esr helps support high peak currents, it also presents a problem during the charge cycle. When the supply voltage is first applied to an uncharged super capacitor, it looks like a low value resistor (esr). This results in a large in-rush current if it is not controlled or limited. Therefore, whenever designers use a super capacitor, they must limit in-rush current.

Several possible solutions are available. The simplest approach is to use a series resistor. In a PC Card the maximum current that can be drawn prior to successful Host/Card negotiation is 70 mA. Assuming that the PC Card controller needs half that current to perform the negotiation, then at power-up the super capacitor must either be disconnected from the supply or current limited using an $\sim 100\Omega$ resistor ($R=V/I$). At that rate the capacitor will be fully charged in approximately 6.7 minutes (assuming the capacitors is fully charged in approximately 5 time constants).

In a second, more practical approach, designers can allow the PC Card to source more power after the successful negotiation between the host and the card. They can then use a lower value resistor to increase the charging current. Initially the voltage of the capacitor is still low and the power dissipation in the resistor will be very high. As the capacitor starts to charge and the voltage starts to rise, the power dissipation reduces and the resistor value can be decreased.

In figure 1 below, a sample circuit comprised of a series of decreasing resistor values is switched in during the capacitor charging cycle. It is important to note two important potential problems with this approach. First, timing of the switching points must be precisely timed, which requires either very accurate and expensive resistors or monitoring by several additional voltage detectors. Second, when the capacitor is fully charged and the PC Card is removed, the energy stored in the capacitor might be high enough to damage the connector pin.

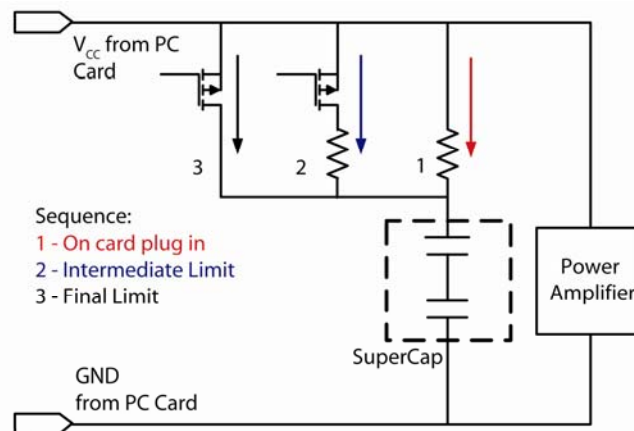


Figure 1: Resistive Charging Sequence

PC Card		
Voltage	Current Level 0 (max)	Current Level 1 (max)
3.3V ± 10%	70mA	1000mA
5.0V ± 10%	100mA	1000mA
CF Card		
Voltage	Current Level 0 (max)	Current Level 1 (max)
3.3V ± 5%	75mA	500mA
5.0V ± 10%	100mA	500mA
USB Port		
Voltage	Current Level 0 (max)	Current Level 1 (max)
5.0V ± 10%	100mA	500 mA

Figure 2: Maximum Currents

As a third option, designers can charge the super capacitor using an industry-standard current-limiting smartswitch. These devices use an integrated P or N channel MOSFET as a load switch and integrate additional monitoring and protection circuitry to limit the amount of output current. Most smartswitches feature thermal over-load protection so if the chip temperature exceeds its stated maximum while in current limit, the device will turn off. As the chip cools down, the device will turn back on and thermally oscillate at a low frequency until the period of high dissipation ends. This is the case when charging a super capacitor. This is not a problem since all smartswitches are designed to do this. However, during the time the switch is off, the capacitor is not charging and therefore increasing the time to full charge. Furthermore, without additional circuitry there is no way to detect when the capacitor is fully charged and tell the system that it is ready to start transmitting.

New Approach

Recently power semiconductor designers have developed a new type of device which overcomes the problems associated with safely charging a super capacitor. The first example of these new devices is the AAT4620 from Advanced Analogic Technologies (AnalogicTech). This current-limited smartswitch integrates all the circuitry required to limit current, protect the PC Card connector, continuously charge the capacitor, notify when the system is ready for use, and determine when to start recharging the capacitor. To help minimize system footprint, the AAT4620 squeezes all of these functions into a tiny 12-pin TSOPJW package which occupies less than 9mm² of PCB.

Figure 3 below illustrates a typical application diagram using the AAT4620 smartswitch. The two externally programmable current limits on the device can be used to provide different limits during the host/card negotiation. When the AAT4620 powers up, it provides a low resistance path between the supply and the super capacitor. If thermal dissipation is low, the device eventually will enter current limit and the capacitor will continue to charge until it gets to within 50mV (or 5.5V) of its final value and the charging switch turns off. When the capacitor gets to within 98% of its final value, an internal comparator senses the voltage and delivers a ready signal to alert the external microcontroller that transmission can begin.

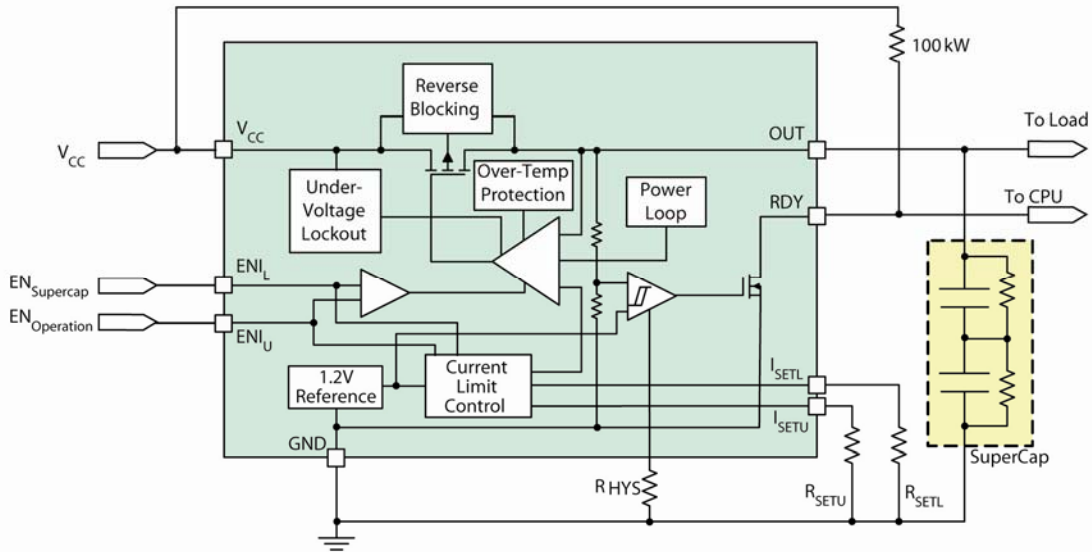


Figure 3: AAT4620 Application Example

When heat dissipation is high, the AAT4620's temperature will rapidly rise until it reaches an internally programmed limit. At this point, the device's integrated digital power loop initiates. This function regulates the die temperature to about 100 degree C by sensing the die temperature at regular intervals and increasing or decreasing the current by 1/32 of the current limit set point. This ability to control the die temperature helps protect the device from damage and minimizes charge time by ensuring that the super capacitor is charging at all times.

Typically designers size the super capacitor to minimize the voltage droop during transmission and allow recharging during the receive phase. The AAT4620 adds adjustable hysteresis which allows the user to set a point at which the super capacitor is topped off. This level can be set at any value ranging from 200 mV less than full charge to zero.

Conclusion

Until recently designers of portable systems have rarely used super capacitors for applications other than back-up or standby functions where currents are low and charge times are fairly long. But a growing range of new applications, led by a new generation of high performance data cards, demand high peak currents that are forcing designers to consider new solutions.

In these applications designers are frequently turning to super capacitors to deliver these high currents as long as they can find ways to minimize charge time and maintain a small solution size. By integrating all the circuitry required to limit current, protect the PC card connector, continuously charge the capacitor, and notify the system when the capacitor is ready for use, a new generation of smart switches promises to simplify design using super capacitors while minimizing component count and reducing system size.

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